AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method for fabricating a detector [[(50)]] having a plurality of pixels [[(31)]] each including a sensor element coupled to a sensor input [[(32)]] of an electronic processing circuit [[(34)]], the method comprising:

integrating the electronic processing circuits on a CMOS wafer by stitching a plurality of reticles [[(26, 27, 28)]] of at least two different types so as to form an integrated circuit having an array of electronic processing circuits each having a respective sensor input disposed toward a first surface of the wafer and accessible from the first surface via a terminal pad [[(36)]] formed near an edge of the integrated circuit such that each terminal pad serves to access multiple sensor inputs via a controller [[(35)]] fabricated at an edge of the wafer; [[and]]

disposing the sensor elements on the first surface of the respective integrated circuits in said detector whereby an exposed surface of the sensor elements forms a common first electrode towards which incident photons are directed, and an opposite unexposed surface thereof forms multiple second electrodes of opposite polarity to the first electrode each in registration with a corresponding sensor input; [[.]]

integrating the electronic processing circuits on a plurality of rectangular IC modules each having a major edge and a minor edge, the major edge having a dimension (L) that is substantially half of a width of the detector, such that said terminal pads are formed towards a minor edge of the IC module; and

juxtaposing multiple pairs of said IC modules edge to edge so that respective minor edges of each of pair are juxtaposed with the respective terminal pads of each IC module disposed toward opposing outer non-contiguous edges of the detector and with adjacent pairs of IC modules being juxtaposed along their major edges;

the sensor elements being disposed on the first surface of the respective IC modules in said detector.

2. (Canceled)

3. (Previously presented) The method according to claim 1, wherein disposing the sensor elements includes growing on the first surface of the wafer amorphous or polycrystalline sensor material that is capable of detecting incident photons directly.

4. (Original) The method according to claim 3, the amorphous or polycrystalline sensor material is mercuric iodide.

5. (Currently amended) The method according to claim 1, further including mounting the detector assembly on a PCB [[(57)]] prior to disposing the sensor elements.

6. (Currently amended) The method according to claim 1, ~~when used to fabricate~~ wherein the detector forms part of a sensor array for a high energy photon imaging detector.

7. (Currently amended) A detector assembly manufactured according to the method of claim 1.

8. (Currently amended) A detector assembly [[(50)]] having a plurality of pixels [[(31)]] that include a sensor element coupled to a sensor input [[(32)]] of an electronic processing circuit [[(34)]], the detector assembly comprising:

at least one integrated circuit [[(40)]] formed by stitching a plurality of reticles of at least two different types and having an array of electronic processing circuits each having a respective sensor input disposed toward a first surface of the wafer and accessible from the first surface via a terminal pad [[(36)]] formed near an edge of the integrated circuit such that each terminal pad serves to access multiple sensor inputs via a controller [[(35)]] fabricated at an edge of the wafer; [[and]]

sensor elements [[(56)]] disposed on the first surface of the at least one integrated circuit in said detector assembly whereby an exposed surface of the sensor elements forms a common first electrode towards which incident photons are directed, and an opposite unexposed surface thereof forms multiple second electrodes of opposite polarity to the first electrode each in registration with a corresponding sensor input; [[.]]

a plurality of rectangular IC modules each fabricated on a very large area CMOS wafer and having a major edge and a minor edge, the major edge having a dimension (L) that is substantially half of a width of the detector, the IC module having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input disposed toward a first surface of the wafer and accessible from the first surface via a terminal pad formed towards a minor edge of the IC module such that each terminal pad serves to access multiple sensor inputs via a controller fabricated at an edge of the wafer; and

multiple pairs of IC modules juxtaposed edge to edge so that respective minor edges of each of pair are juxtaposed with the respective terminal pads of each IC module disposed toward opposing outer non-contiguous edges of the detector and with adjacent pairs of IC modules being juxtaposed along their major edges;

the sensor elements being disposed on the first surface of the respective IC modules in said detector assembly.

9. (Canceled)

10. (Previously presented) The detector assembly according to claim 8, wherein the sensor elements include amorphous or polycrystalline sensor material grown on the first surface of the wafer and being capable of detecting incident photons directly.

11. (Previously presented) The detector assembly according to claim 8, wherein the sensor elements include monolithically integrated crystalline sensors mounted on the first surface of the wafer in registration with respective sensor inputs.

12. (Currently Amended) The detector assembly according to claim 8, [[being]] wherein the detector is configured for use in a high energy photon imaging detector.

13. (Currently amended) An IC module for use in manufacture of the detector assembly according to claim 8, the IC module comprising:

a very large area rectangular CMOS wafer [[(30)]] having a major edge and a minor edge, the major having a dimension (L) that is substantially half of a width of the detector and having at least one array of electronic processing circuits each electronic processing circuit having a respective

sensor input disposed toward a first surface of the wafer and accessible from the first surface via a terminal pad [[(36)]] formed towards a minor edge of the sensor array such that each terminal pad serves to access multiple sensor inputs via a controller [[(35)]] fabricated at an edge of the wafer.

14. (Previously presented) The sensor array according to claim 13, further including sensor material deposited on the first surface thereof.